University of Larbi Ben M'Hidi, Oum El Bouaghi
1st year Mathematics + Mathematics and computer Science
Module: **Machine Structure 2** 2023/2024

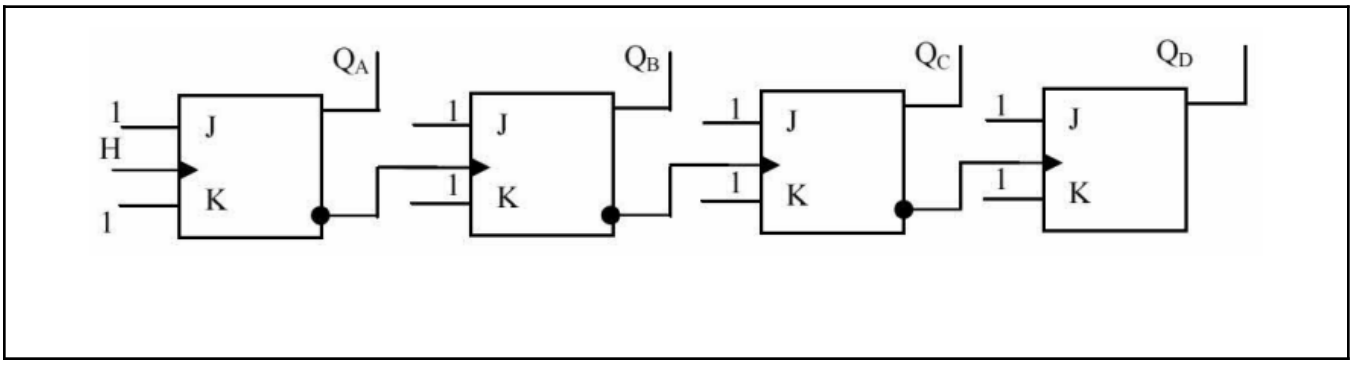
First Name: ……...….
Last Name: ……...…..
Group: …….....

Solution of the 2nd Written Examination

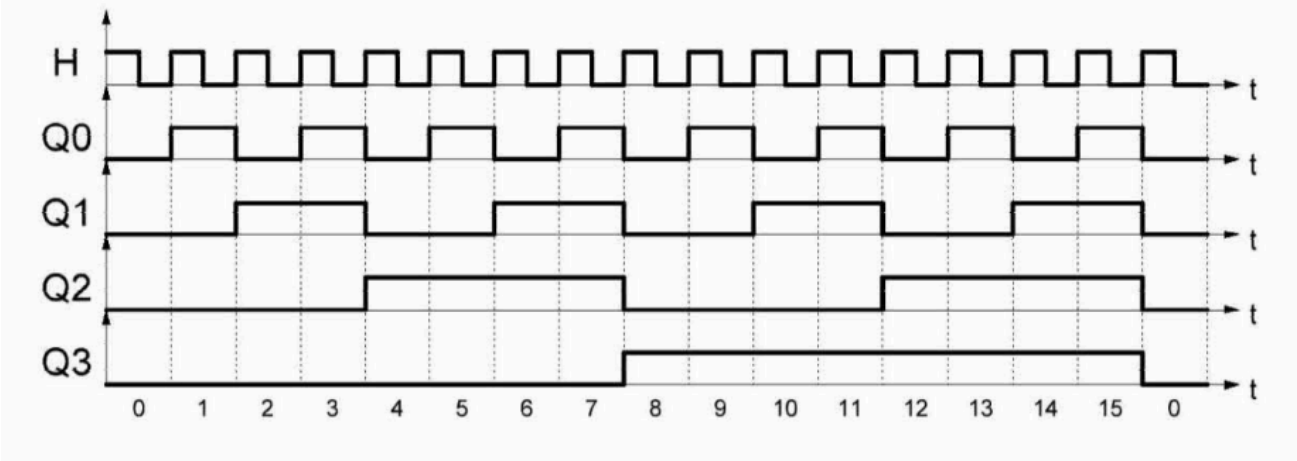
Exercise:

We want to create **a modulo 16 asynchronous counter** using a **JK latch** activated on a **rising edge**.

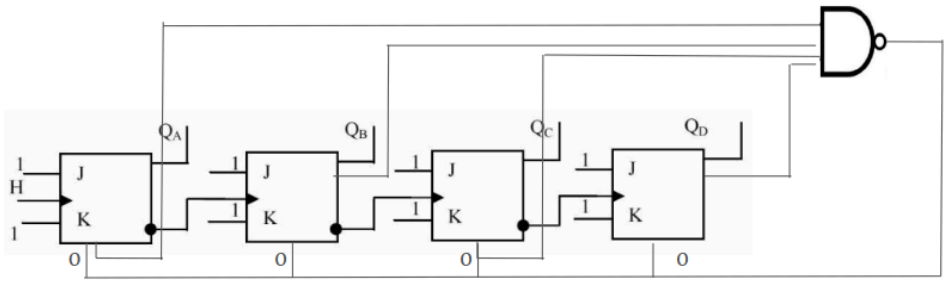
1. Propose a symbolic diagram allowing the creation of this counter using 4 latches (Q_A ,Q_B Q_C ,Q_D).



2. Outline and complete the chronogram related to the proposed implementation in question 1.



Consider the following implementation:



3. Deduce the role of this implementation by justifying the objective of using JK latches.

- This circuit is an asynchronous counter modulo 10. It counts from 0 to 9.
- The objective of using a JK flip-flop is to enable it to be locked in a specific value by forcing both its PRE and CLK inputs to be either 0 or 1.

4. How can we modify this implementation to have an asynchronous down counter module 10.

   There are two methods to achieve down counter from a counter:

   - By changing the synchronization mode from a rising edge mode to a descending edge mode. (figure 1)
   - By modifying the synchronization signal: each latch is synchronized by the resulting signal from the previous latch.

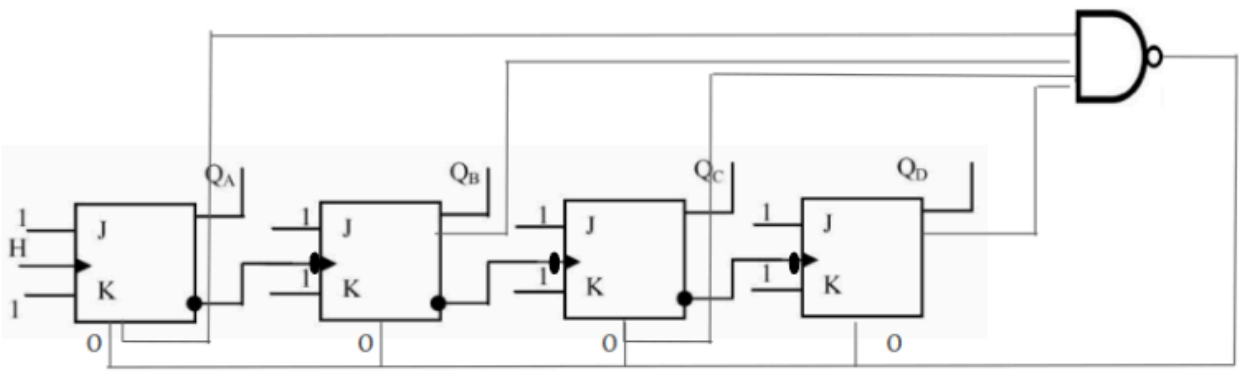


Figure 1

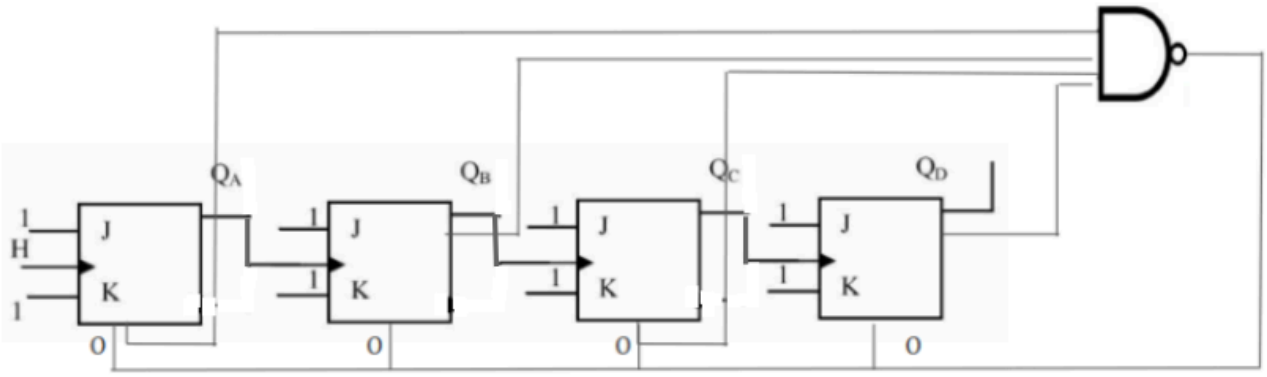


Figure 2