Sequential Logic

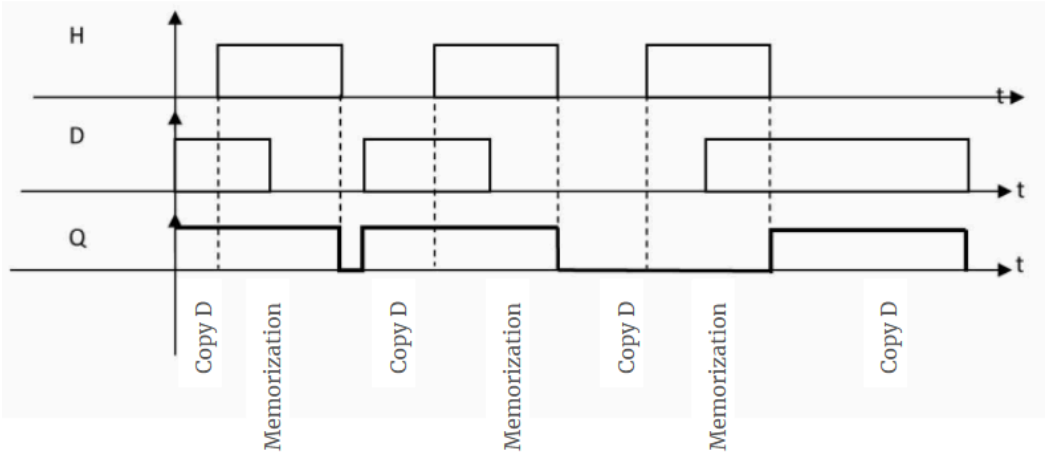
Tutorial: First session

Exercise 1

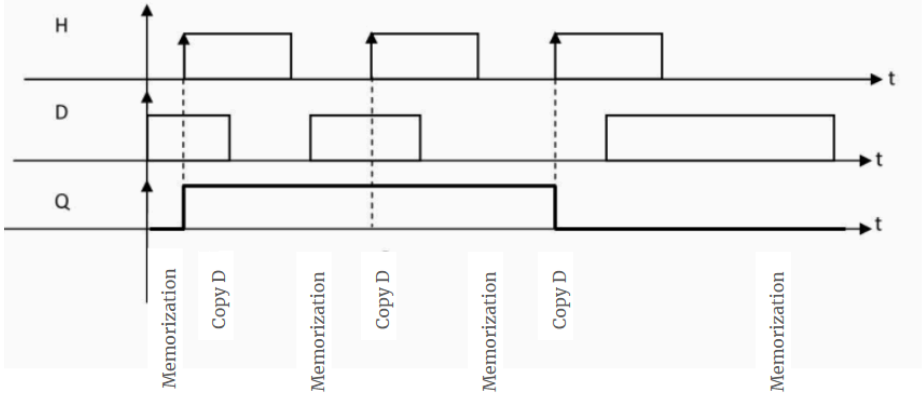
The exercise is designed as a review, and the solution has already been discussed in the course session. (Refer to the course materials for further details.)

Exercise 2

Latch D/ Low level of H

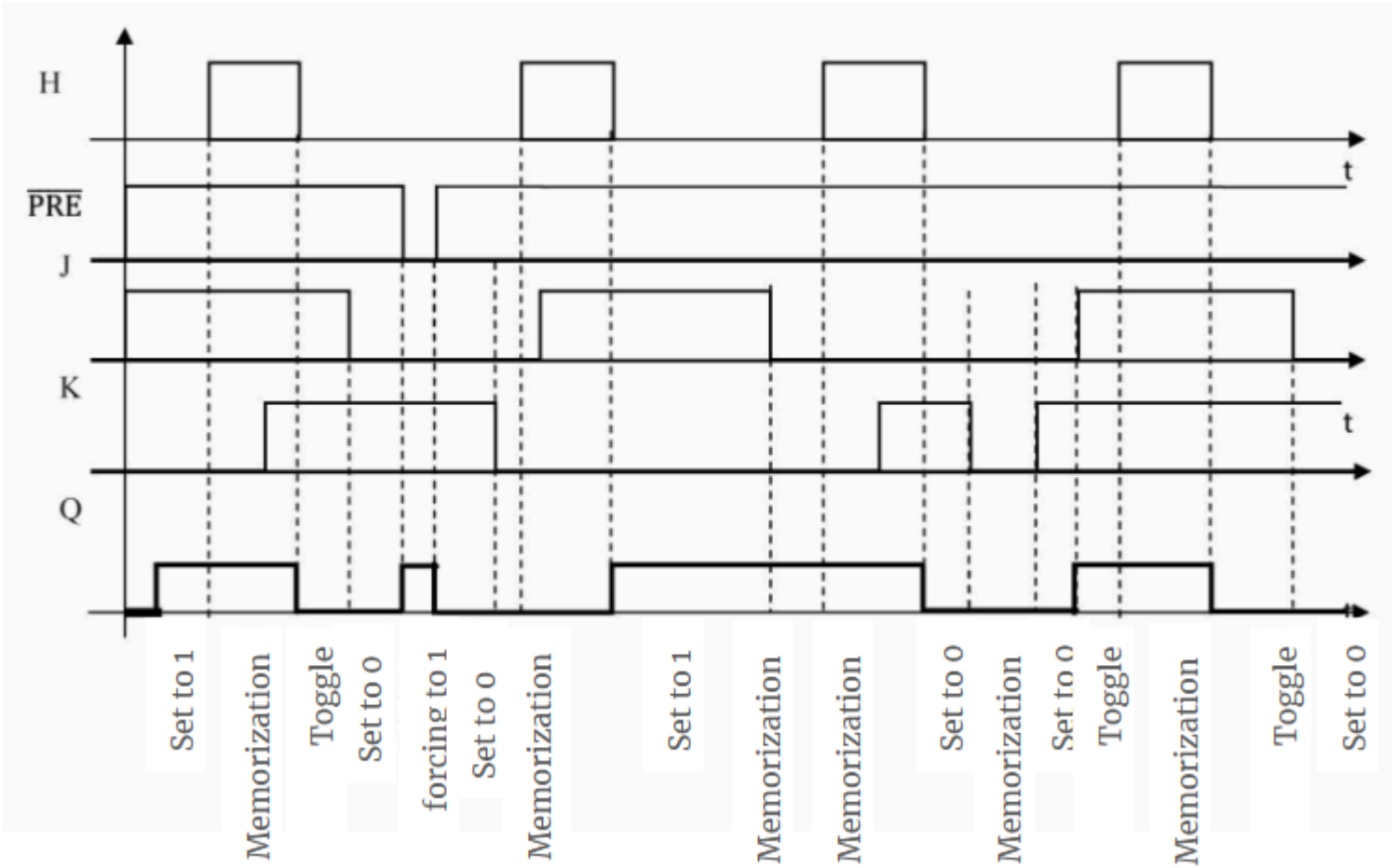


Latch D/ Rising edge of H

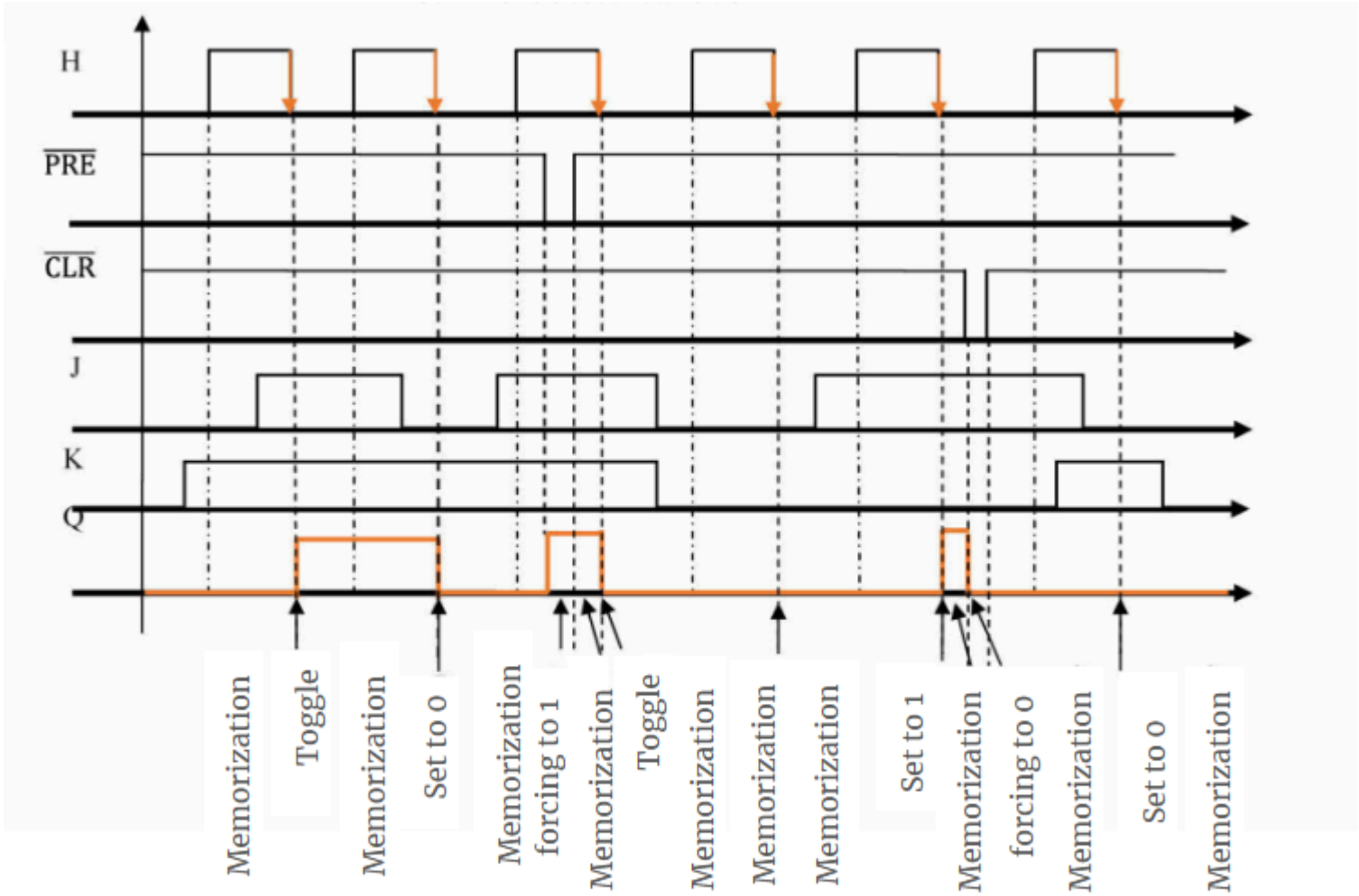


Exercise 3

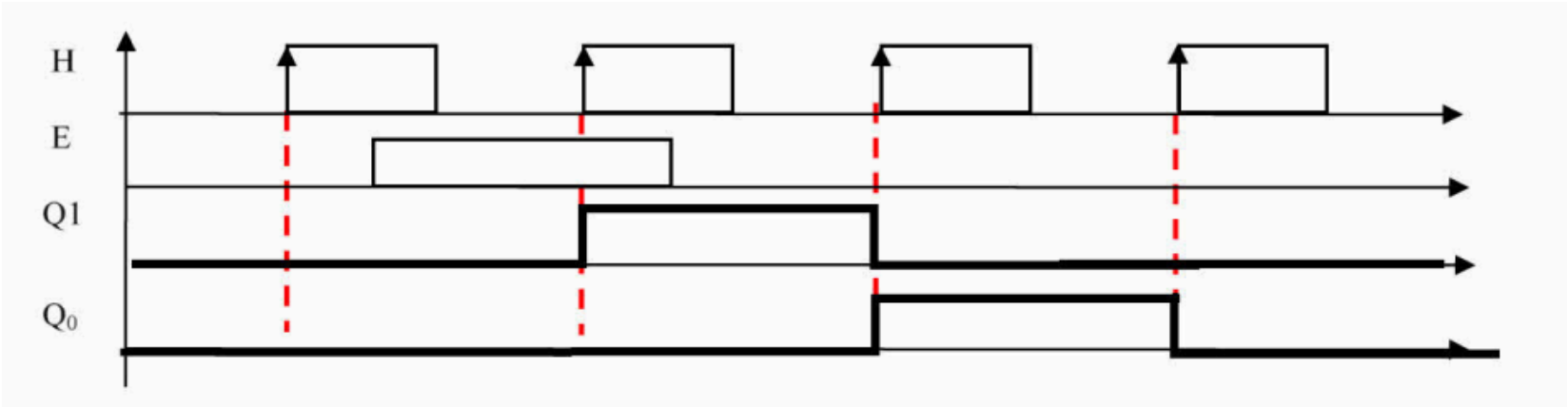
Latch JK / Low level of H



Latch D/ Descending edge of H

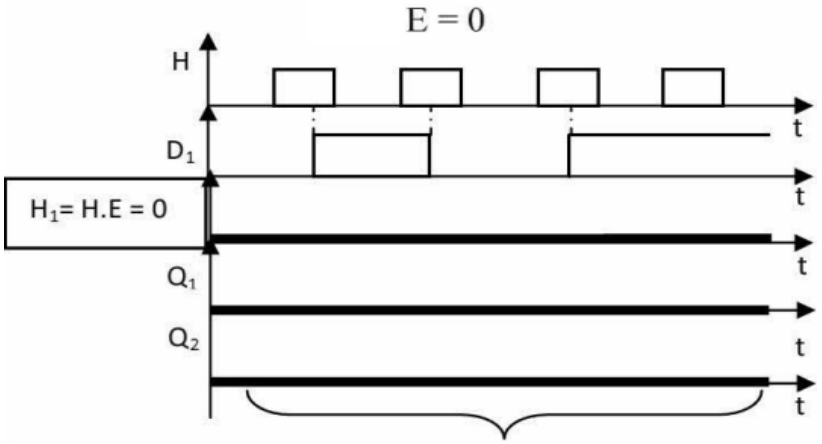


Exercise 4:

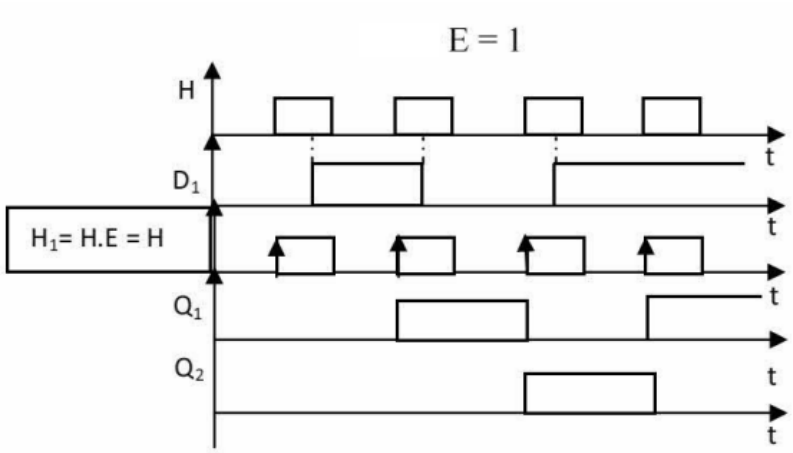


It is a 2-bit left shifting register.

Exercise 5:

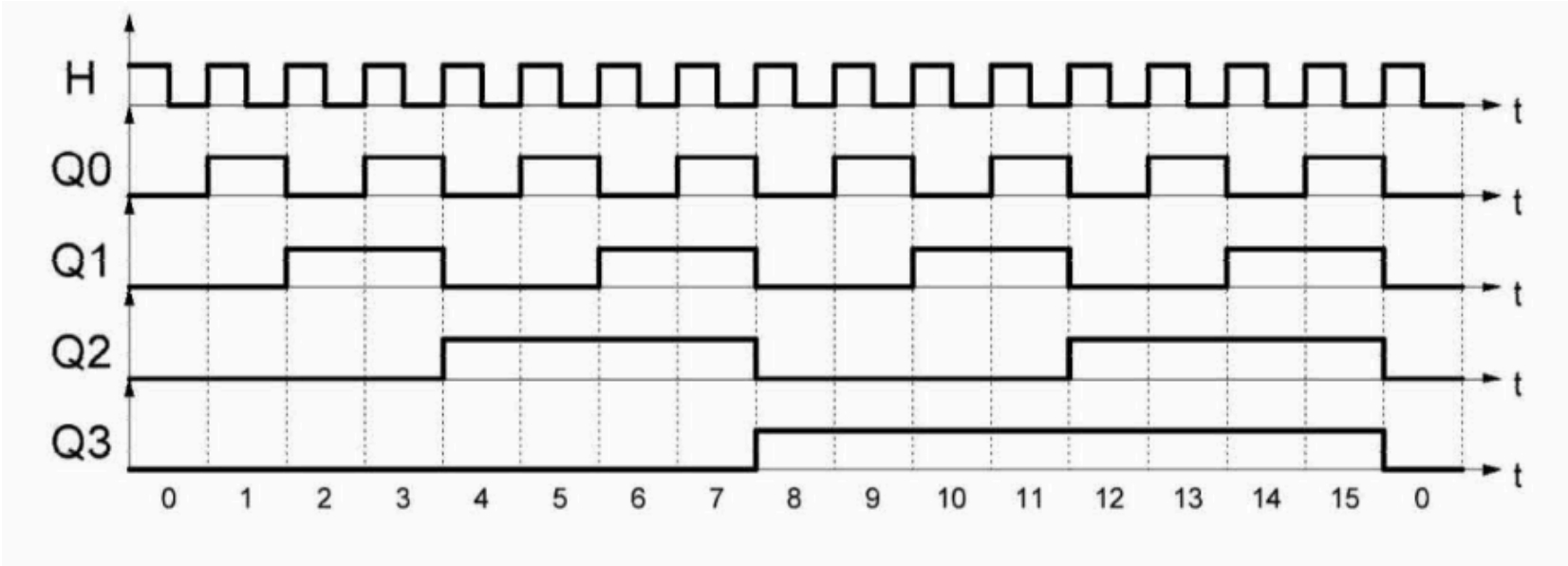


Memorization



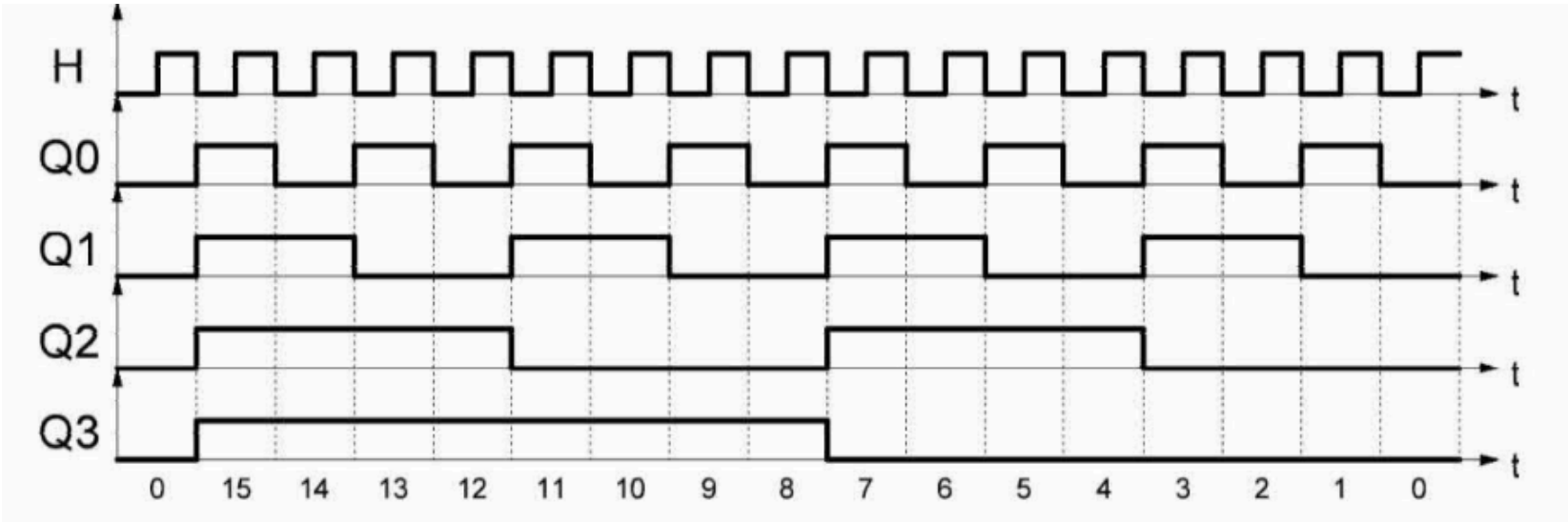
2- In the case E=0, the circuit functions as a storage register
In the case E=1, the circuit functions as a right shift register

Exercise 6



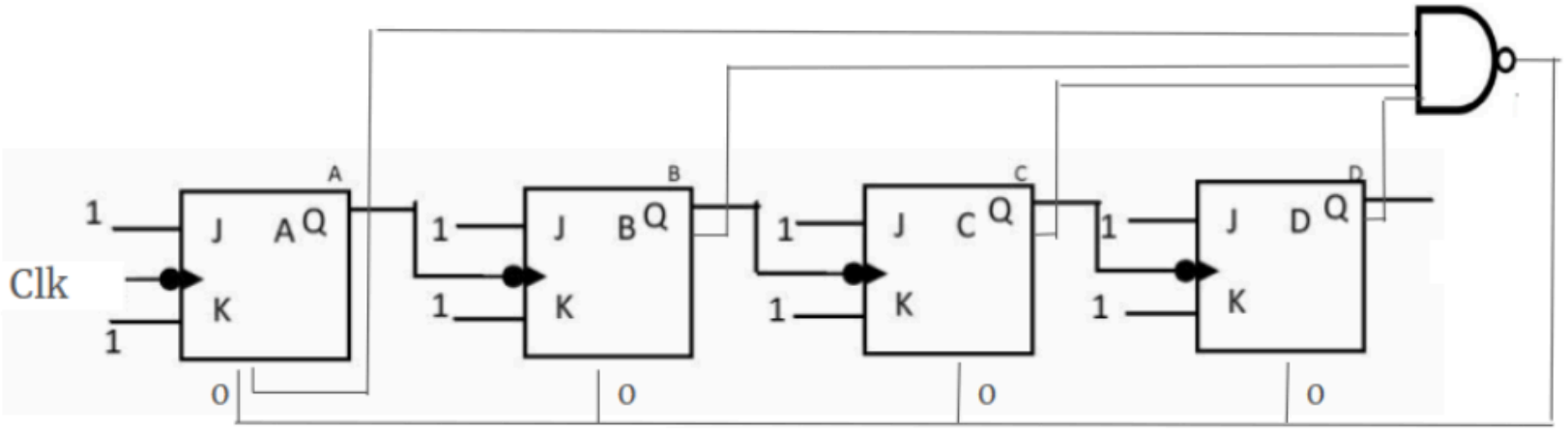
This circuit is an asynchronous counter modulo 16. It counts from 0 to 15

The gate NAND is used to detect the value 12 and replace it with the value 0 => the new circuit is an asynchronous counter modulo 12. It counts from 0 to 11.

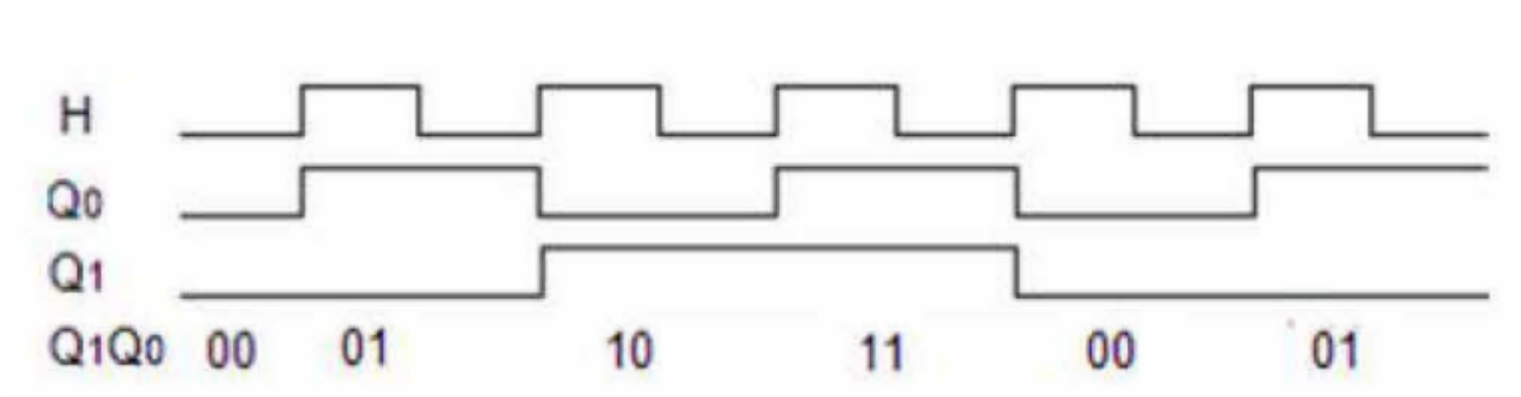


This circuit is a modulo 16 asynchronous decrement counter. It countdown from 15 to 0.

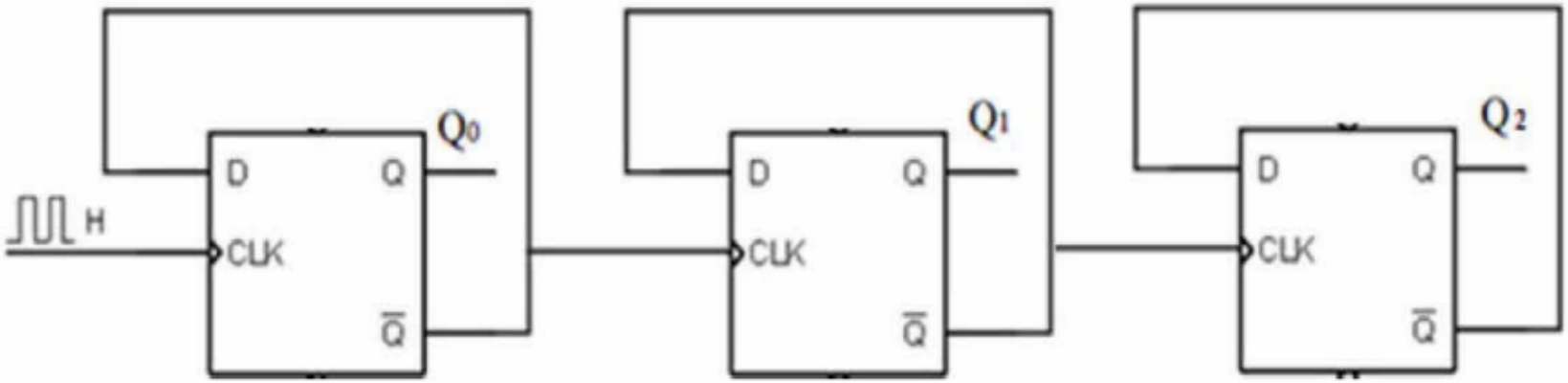
4-

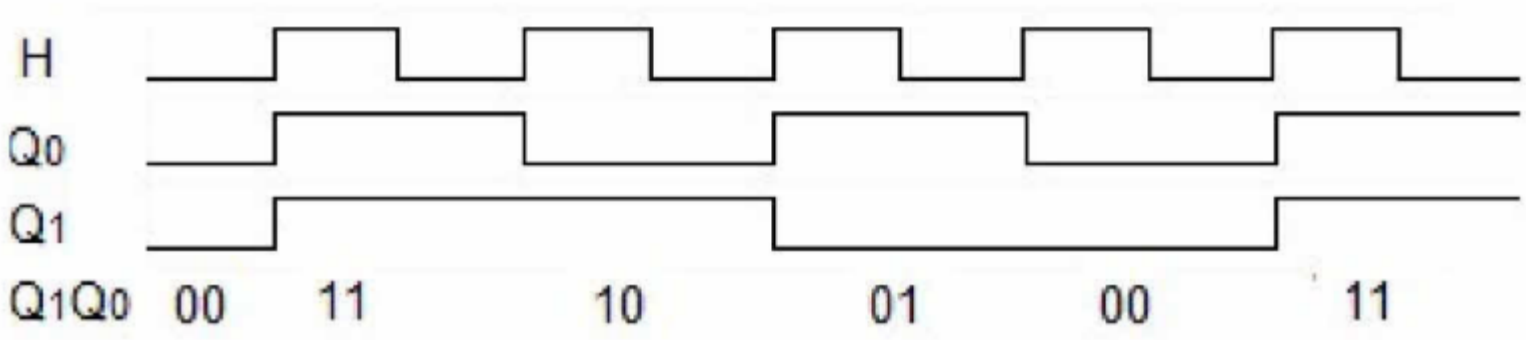


Exercise 7



The obtained sequence : 0-1-2-3-0 => we have a modulo 04 asynchronous counter.





4- The obtained sequence : 0-3-2-1-0 => we have a modulo 04 asynchronous decrement counter.