Combinatorial logic
Exercise series 02

Exercise 1

Make the full adder of a step i using Half Adders.

Exercise 2

Using a 3 select (address) line multiplexer (MUX), perform the following function:

$$F(A,B,C) = \bar{A}B\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}BCD + A\bar{B}CD + AB\bar{C}D + ABC\bar{D} + A\bar{B}\bar{C}\bar{D}$$

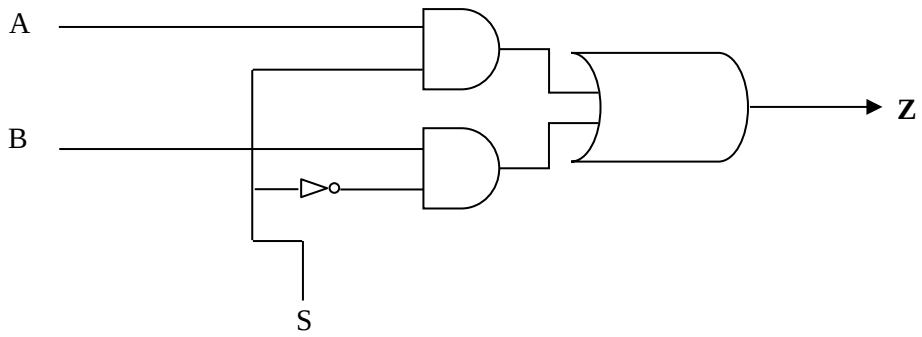
Exercise 3

Consider two 4-bit binary numbers, A($a_3\, a_2\, a_1\, a_0$) and B($b_3\, b_2\, b_1\, b_0$).

1. Give the general diagram of the full adder and the half adder which performs the sum between two bits (a_i and b_i).
2. Give the general diagram of the circuit which adds the two numbers A and B using full adders only.
3. Give the general diagram of the circuit which adds the two numbers A and B using a half adder and 3 full adders.

Exercise 4

Consider the following diagram:



1. Give the expression Z for this circuit and determine its role.
2. Directly create the circuit which makes the choice between two numbers X and Y such that each of them is represented on 4 bits.

Exercise 5

1. Give the truth table of the combinatorial circuit which makes the transformation of a number written in a *BCD* code X(x3x2x1x0) to a number written in the 7-segment code (see the figure).
2. Simplify the function corresponding to segment **(a)** .
3. Represent the circuit corresponding to the simplified function.