Combinational Logic

Tutorial: First session	
Question	**Solution**
Q1	The solution of Q1 is provided in the attached file titled "Q1 Solution". Feel free to check the attachment for the complete solution.
Q2	➔ **Combinational Logic Circuits:** Functionality: Combinational circuits perform operations based solely on the current input values. No Memory: They do not have memory elements, and the output is determined only by the current input values. Immediate Output: The output is immediately produced as a function of the inputs, without considering any past states. **Example**: Logic gates, adders, multiplexers, etc. ➔ **Sequential Logic Circuits:** Functionality: Sequential circuits take into account both the current input values and the past states or inputs. Memory: They include memory elements (typically flip-flops) that store information about past inputs. Timing: The output is dependent not only on the current inputs but also on the order and timing of these inputs. **Example**: Flip-flop-based circuits, counters, registers, memory units, etc.
Q3	Circuit 1: It is observed that the output of this circuit is fed back into the input. Consequently, the output is influenced not only by the 'Write' and 'Data' inputs but also by its previous state. This observation establishes that the circuit is not purely a combinational logic circuit; rather, it exhibits the characteristics of a sequential logic circuit. Circuit 2: Similar to the observation made for Circuit 1, the outputs are explicitly fed back as inputs. This characteristic distinguishes it from a combinational logic circuit, confirming its classification as a sequential circuit. Circuit 3 : In this circuit, the outputs Si (where i ranges from 0 to 3) all depend solely on the inputs 'e_0' and 'e_1'. We can even deduce the equations for these outputs. For example, $S_3 = e_1.e_0$. It can be inferred that this is **a combinational logic circuit.**

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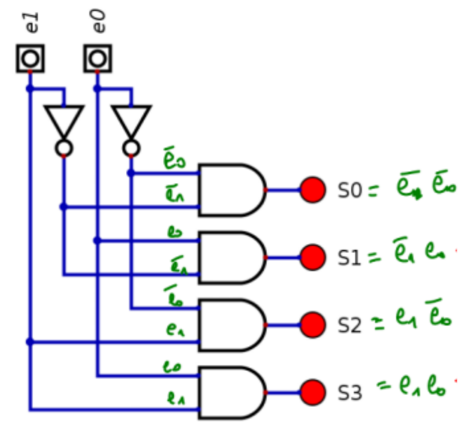
Q4

➔ The analysis of a logic circuit assumes access to its logic diagram, requiring deduction of its functionality. In essence, this involves identifying the equations governing its outputs, potentially simplifying them, and endeavoring to interpret its overall function.

➔ The synthesis takes a reverse approach. It begins with the specification of a problem, aiming to discover a logic circuit diagram that addresses the issue at hand. Hence, in synthesis, the objective is to ultimately derive the logic diagram.

Q5



Tutorial: Session Two

Exercise 2

Upon reading the statement of our problem, we observe that we have only one output (function) to determine. This function indicates an overflow condition during a calculation when it evaluates to "1" and signals the absence of capacity overflow when it evaluates to "0".

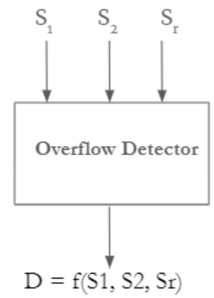
Clearly, it is a boolean function. Let's denote this function as "D".

By analyzing our statement, it's evident that D is contingent on the signs of the two numbers, A and B, involved in a calculation, as well as the sign of the result of this calculation.

- Designate the sign of the first number A as S1.
- Designate the sign of the second number B as S2.
- Designate the sign of the result R as Sr.

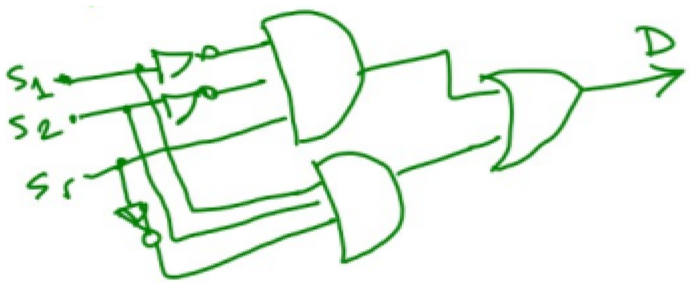
We can, therefore, write: D = f(S1, S2, Sr).

We are indeed dealing with **a logical system**: a Boolean function and Boolean variables.
Let's now find the relationship that exists between the output D and the inputs (S1, S2, Sr).
We will do this by creating a truth table.



	S1	S2	Sr	D	Observation
m_0	0	0	0	0	The sign of A and B is positive and the results are also => no overflow
m_1	0	0	1	1	The sign of A and B is positive and the results is negative => overflow
m_2	0	1	0	0	The sign of A is different from that of b => impossible to have an overflow
m_3	0	1	1	0	The sign of A is different from that of b => impossible to have an overflow
m_4	1	0	0	0	The sign of A is different from that of b => impossible to have an overflow
m_5	1	0	1	0	The sign of A is different from that of b => impossible to have an overflow
m_6	1	1	0	1	The sign of A and B is negative and the results is positive=> overflow
m_7	1	1	1	0	The sign of A and B is negative and the results are also => no overflow

From the truth table, we can deduce the equation of the function D, $D=\sum(1,6)$.
$D= \overline{S_1}.\overline{S_2}.S_r + S_1.S_2.\overline{S_r}$



Exercise 3

Truth Table

a1	a0	b1	b0	S1	S0	C
0	0	0	0	0	0	0
0	0	0	1	0	1	0
0	0	1	0	1	0	0
0	0	1	1	1	1	0
0	1	0	0	0	1	0
0	1	0	1	1	0	0
0	1	1	0	1	1	0
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	1	0
1	0	1	0	0	0	1
1	0	1	1	0	1	1
1	1	0	0	1	1	0
1	1	0	1	0	0	1
1	1	1	0	0	1	1
1	1	1	1	1	0	1

Logical expressions

$S_1 = \Sigma(2,3,5,6,8,9,12,15)$

$S_0 = \Sigma(1,3,4,6,9,11,12,14)$

$C = \Sigma(7,10,11,13,14,15)$

Simplification

$S_1 = \Sigma(2,3,5,6,8,9,12,15)$

b1b0 \ a1a0	00	01	11	10
00	0	0	1	1
01	0	1	0	1
11	1	0	1	0
10	1	1	0	0

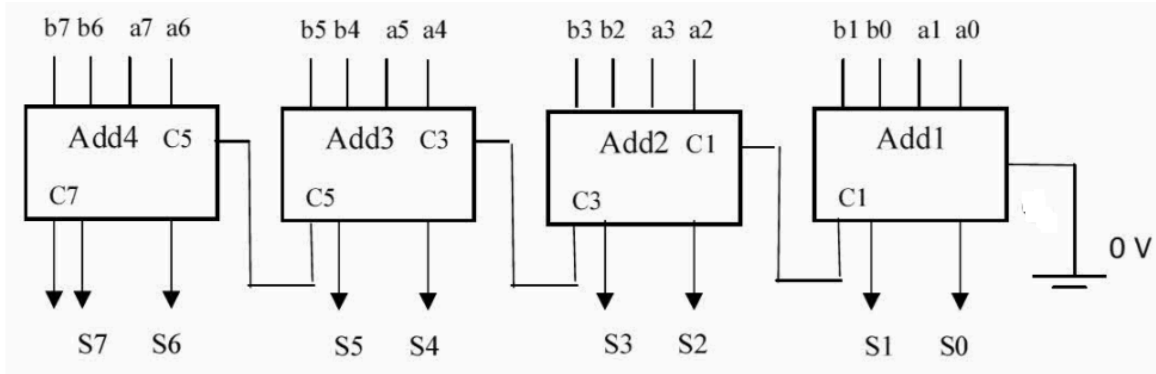
$$S_1 = a_1\overline{b_1}\overline{b_0} + a_1\overline{a_0}\overline{b_1} + \overline{a_1}\,\overline{a_0}b_1 + \overline{a_1}b_1\overline{b_0} + \overline{a_1}a_0\overline{b_1}b_0 + a_1a_0b_1b_0$$

$$S_1 = a_0b_0 \oplus a_1 \oplus b_1$$

$$S_0 = \overline{a_0}b_0 + a_0\overline{b_0} = a_0 \oplus b_0$$

$$C = a_1a_0b_0 + b_0b_1a_0 + a_1b_1 = b_0a_0(b_1 + a_1) + b_1a_1$$

Q2



Exercise 4

Truth Table and Logical expressions

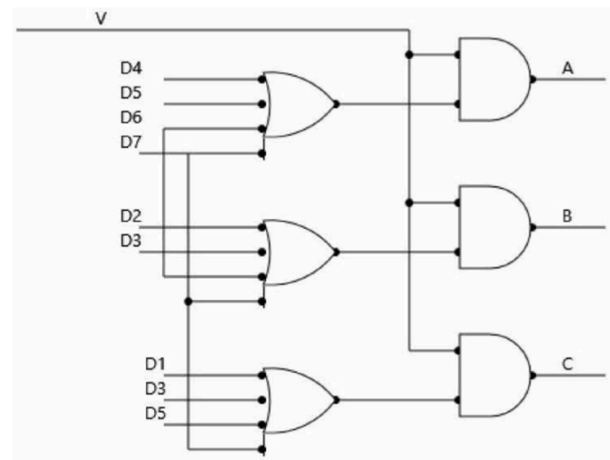
V	D7	D6	D5	D4	D3	D2	D1	D0	A	B	C
0	x	x	x	x	x	x	x	x	0	0	0
1	0	0	0	0	0	0	0	1	0	0	0
1	0	0	0	0	0	0	1	0	0	0	1
1	0	0	0	0	0	1	0	0	0	1	0
1	0	0	0	0	1	0	0	0	0	1	1
1	0	0	0	1	0	0	0	0	1	0	0
1	0	0	1	0	0	0	0	0	1	0	1
1	0	1	0	0	0	0	0	0	1	1	0
1	1	0	0	0	0	0	0	0	1	1	1

$$A = V(D_4 + D_5 + D_6 + D_7)$$

$$B = V(D_2 + D_3 + D_6 + D_7)$$

$$C = V(D_1 + D_3 + D_5 + D_7)$$

Logigram



Exercise 5

Dec	A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	0
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1

<u>a</u>

AB \ CD	00	01	11	10
00	1	0	1	1
01	0	1	1	1
11	X	X	X	X
10	1	1	X	X

$$a = A + C + \overline{B \oplus D}$$

With same method, we can found:

$$b = \bar{B} + (\overline{C \oplus D})$$

$$c = \bar{C} + D + B$$

$$d = A + C\bar{D} + (B \oplus \bar{C}D)$$

$$e = \bar{D}(C + \bar{B})$$

$$f = A + \bar{C}\bar{D} + B(\bar{C} + \bar{D})$$

$$g = (B \oplus C) + A\bar{C} + C\bar{D}$$

Third Tutorial Session

Exercise 6

Q1: This circuit features **8 inputs** to **a single output** and incorporates **3 address lines** for the 8 input lines, making it **a multiplexer (MUX 8 to 1)**. where:

- d_0 to d_7: Input lines
- y: Output
- A_0, A_1, A_2: Address lines
- E: Enable input, active at a low level.

Q2+Q3: Truth Table and the Logigram

Q4:

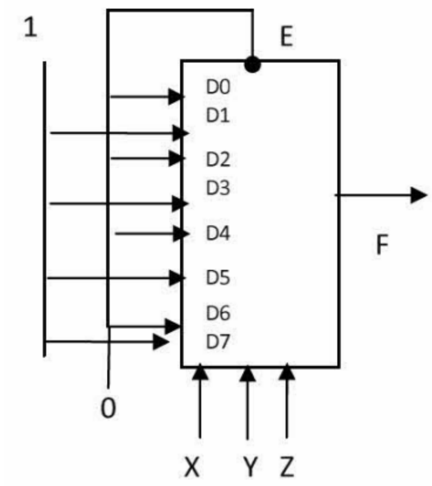
Q5

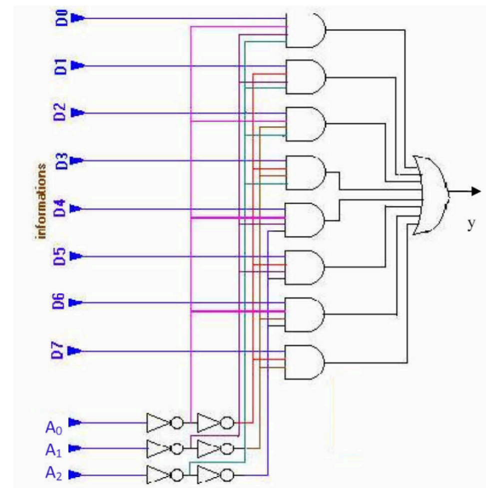
E	A2	A1	A0	Y
1	X	X	X	0
0	0	0	0	d0
0	0	0	1	d1
0	0	1	0	d2
0	0	1	1	d3
0	1	0	0	d4
0	1	0	1	d5
0	1	1	0	d6
0	1	1	1	d7

$$y = \bar{E}[(\overline{A_2}\,\overline{A_1}\,\overline{A_0})d_0 + (\overline{A_2}\,\overline{A_1}A_0)d_1 + (\overline{A_2}A_1\overline{A_0})d_2 + (\overline{A_2}A_1A_0)d_3 + (A_2\overline{A_1}\,\overline{A_0})d_4 + (A_2\overline{A_1}A_0)d_5 + (A_2A_1\overline{A_0})d_6 + (A_2A_1A_0)d_7]$$

$$F(x,y,z) = \Sigma(1,3,5,7)$$

x	y	z	f	di
0	0	0	0	d0 = 0
0	0	1	1	d1 = 1
0	1	0	0	d2 = 0
0	1	1	1	d3 = 1
1	0	0	0	d4 = 0
1	0	1	1	d5 = 1
1	1	0	0	d6 = 0
1	1	1	1	d7 = 1



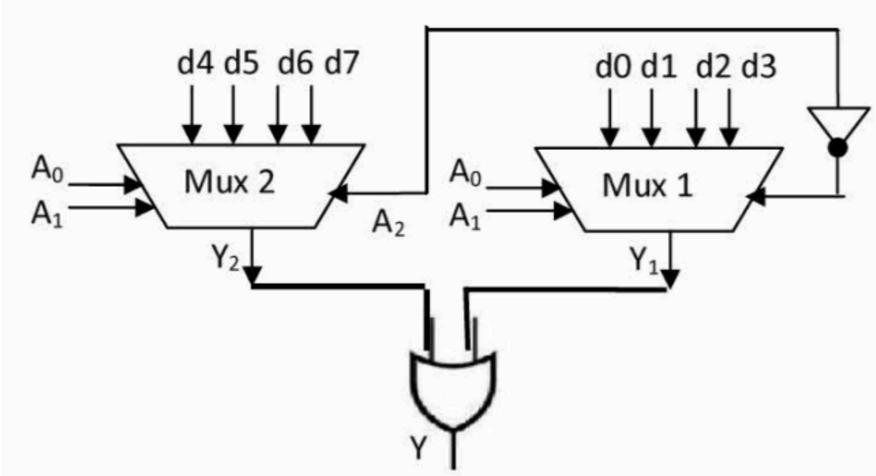


Q5: We need two 4x1 Mux to achieve the 8x1 mux. The truth table of an 8x1 MUX will be shared between the two 4x1 MUXes as follows:

validation Link

A2	A1	A0	Y
0	0	0	d0
0	0	1	d1
0	1	0	d2
0	1	1	d3
1	0	0	d4
1	0	1	d5
1	1	0	d6
1	1	1	d7

Rows d0–d3: Mux 4x1 Level 1
Rows d4–d7: Mux 4x1 Level 2



Exercise 7

Q1: The circuit does not function correctly in its current configuration due to having only 3 address lines, which is insufficient to address all 16 outputs. Therefore, an additional fourth address line ($4^2=16$) is required to adequately address all outputs.

Q2: Truth Table:

E	A3	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	...	Y15
1	X	X	X	X	0	0	0	0	0	0	0	0	0		0
0	0	0	0	0	D	0	0	0	0	0	0	0	0		0
0	0	0	0	1	0	D	0	0	0	0	0	0	0		0
0	0	0	1	0	0	0	D	0	0	0	0	0	0		0
0	0	0	1	1	0	0	0	D	0	0	0	0	0		0
0	0	1	0	0	0	0	0	0	D	0	0	0	0		0
0	0	1	0	1	0	0	0	0	0	D	0	0	0		0
0	0	1	1	0	0	0	0	0	0	0	D	0	0		0
0	0	1	1	1	0	0	0	0	0	0	0	D	0		0
0	1	0	0	0	0	0	0	0	0	0	0	0	D	....	0
0	1	0	0	1	0	0	0	0	0	0	0	0	0		0
0	1	0	1	0	0	0	0	0	0	0	0	0	0		0
0	1	0	1	1	0	0	0	0	0	0	0	0	0		0
0	1	1	0	0	0	0	0	0	0	0	0	0	0		0
0	1	1	0	1	0	0	0	0	0	0	0	0	0		0
0	1	1	1	0	0	0	0	0	0	0	0	0	0		0
0	1	1	1	1	0	0	0	0	0	0	0	0	0	....	D

$$y_0 = \bar{E}D(\overline{A_3}\,\overline{A_2}\,\overline{A_1}\,\overline{A_0}) \quad , y_1 = \bar{E}D(\overline{A_3}\,\overline{A_2}\,\overline{A_1}A_0) \quad ,$$

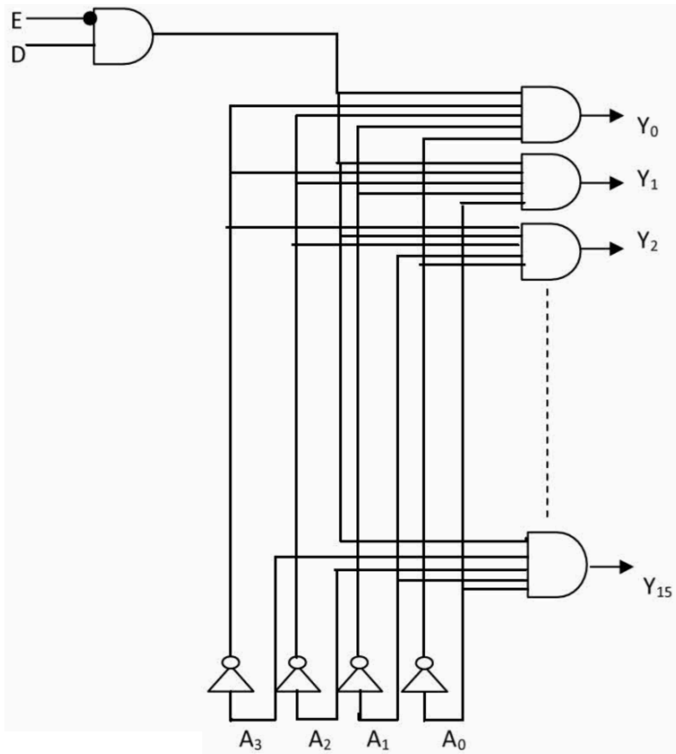
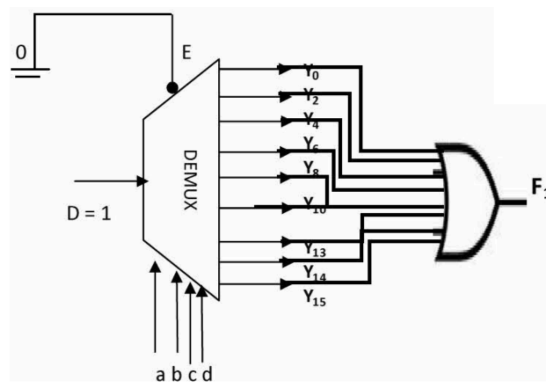
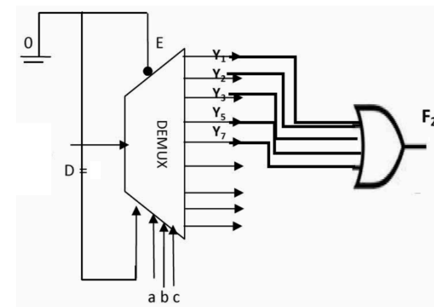
$$y_2 = \bar{E}D(\overline{A_3}\,\overline{A_2}\,A_1\overline{A_0}) \quad , y_3 = \bar{E}D(\overline{A_3}\,\overline{A_2}\,A_1A_0) \quad , y_4 = \bar{E}D(\overline{A_3}\,A_2\overline{A_1}\,\overline{A_0}) \; ,$$

$$y_5 = \bar{E}D(\overline{A_3}\,A_2\overline{A_1}\,A_0) \, , y_6 = \bar{E}D(\overline{A_3}\,A_2\,A_1\overline{A_0}) \quad , y_7 = \bar{E}D(\overline{A_3}\,A_2\,A_1A_0) \, ,$$

$$y_8 = \bar{E}D(A_3\,\overline{A_2}\,\overline{A_1}\,\overline{A_0}) \quad , y_9 = \bar{E}D(A_3\,\overline{A_2}\,\overline{A_1}A_0) \quad , y_{10} = \bar{E}D(A_3\,\overline{A_2}\,A_1\overline{A_0}) \; ,$$

$$y_{11} = \bar{E}D(A_3\,\overline{A_2}\,A_1A_0) \quad , y_{12} = \bar{E}D(A_3\,A_2\overline{A_1}\,\overline{A_0}) \, , y_{13} = \bar{E}D(A_3\,A_2\overline{A_1}\,A_0) \, ,$$

$$y_{14} = \bar{E}D(A_3\,A_2\,A_1\overline{A_0}) \quad , y_{15} = \bar{E}D(A_3\,A_2\,A_1A_0)$$

	Q3: Logigram	**Q4**	**Q5**
		$F_1(a,b,c,d) = \sum(0,2,4,6,8,10,13,14,15)$ 	$F_2(a,b,c) = \sum(1,2,3,5,7)$  **It is important to force the entry of the most significant address to zero**

Exercise 8

Q1:Truth Table

b1	b0	a1	a0	E	I	S
0	0	0	0	1	0	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	0	1	0
0	1	0	1	1	0	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	0	1	0
1	0	0	1	0	1	0
1	0	1	0	1	0	0
1	0	1	1	0	0	1
1	1	0	0	0	1	0
1	1	0	1	0	1	0
1	1	1	0	0	1	0
1	1	1	1	1	0	0

Q2

$$E = \overline{b_1}\,\overline{b_0}\,\overline{a_1}\,\overline{a_0} + \overline{b_1} b_0 \overline{a_1} a_0 + b_1 \overline{b_0} a_1 \overline{a_0} + b_1 b_0 a_1 a_0$$

$$= \overline{b_1}\,\overline{a_1}\left(\overline{b_0}\,\overline{a_0} + b_0 a_0\right) + b_1 a_1\left(\overline{b_0}\,\overline{a_0} + b_0 a_0\right)$$

$$E = \overline{(b_0 \oplus a_0)}.\overline{(b_1 \oplus a_1)}$$

S :

b1b0 \ a1a0	00	01	11	10
00	0	1	1	1
01	0	0	1	1
11	0	0	0	0
10	0	0	1	0

$$S = \overline{b_1} a_1 + \overline{b_0} a_0 (\bar{b}_1 + a_1)$$

I :

b1b0 \ a1a0	00	01	11	10
00	0	0	0	0
01	1	0	0	0
11	1	1	0	1
10	1	1	0	0

$$I = b_1\overline{a_1} + b_1 b_0 \bar{a}_0 + b_0 \bar{a}_1 \bar{a}_0$$

$$I = b_1\bar{a}_1 + b_0\bar{a}_0(b_1 + \overline{a_1})$$

Q3

Draw up the corresponding logigram using two input gates

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Fourth Tutorial Session

Exercise 9

Truth Table

I1	I2	I3	M1	M2
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	1
1	0	0	0	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

$$M_1 = I_1I_2 + I_1I_3 + I_2I_3$$

I1 \ I2 I3	00	01	11	10
0	0	0	1	0
1	0	1	1	1

$$M_2 = I_1 + I_2 + I_3$$

I1 \ I2 I3	00	01	11	10
0	0	1	1	1
1	1	1	1	1

Logigram

NAND based logigram

$$\overline{\overline{M_1}} = \overline{\overline{I_1I_2 + I_1I_3 + I_2I_3}} = \overline{\overline{I_1I_2}.\overline{I_1I_3}.\overline{I_2I_3}}$$

$$\overline{\overline{M_2}} = \overline{\overline{I_1 + I_2 + I_3}} = \overline{\overline{I_1}.\overline{I_2}.\overline{I_3}}$$

NOR based logigram

$$\overline{\overline{M_1}} = \overline{\overline{\overline{\overline{I_1I_2}} + \overline{\overline{I_1I_3}} + \overline{\overline{I_2I_3}}}} = \overline{\overline{\overline{\overline{I_1} + \overline{I_2}} + \overline{\overline{I_1} + \overline{I_3}} + \overline{\overline{I_2} + \overline{I_3}}}}$$

$$\overline{\overline{M_2}} = \overline{\overline{I_1 + I_2 + I_3}}$$