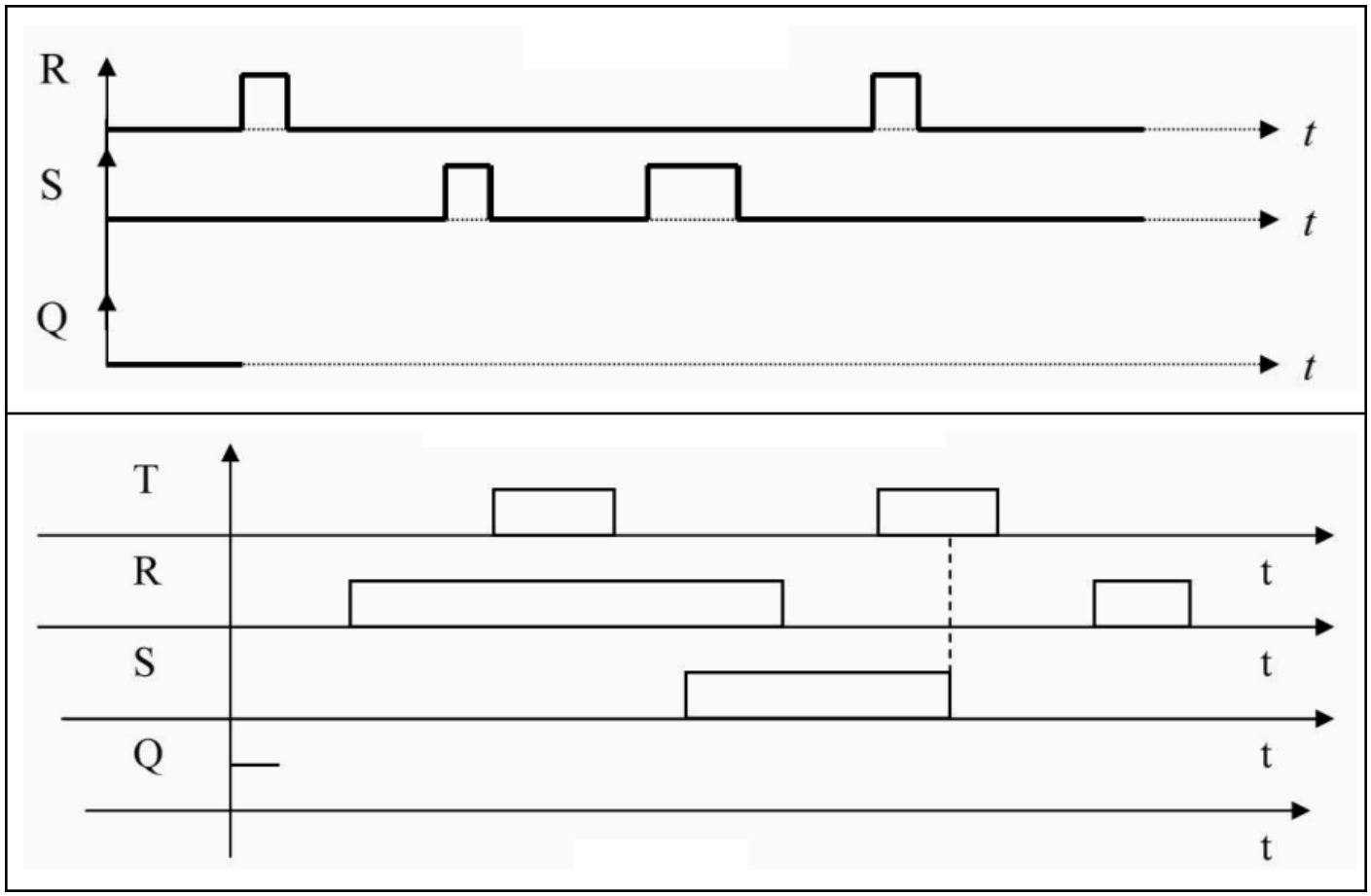
Sequential Logic

Exercise 1:

1- Complete the chronogram (timing diagram) of the RS latch.

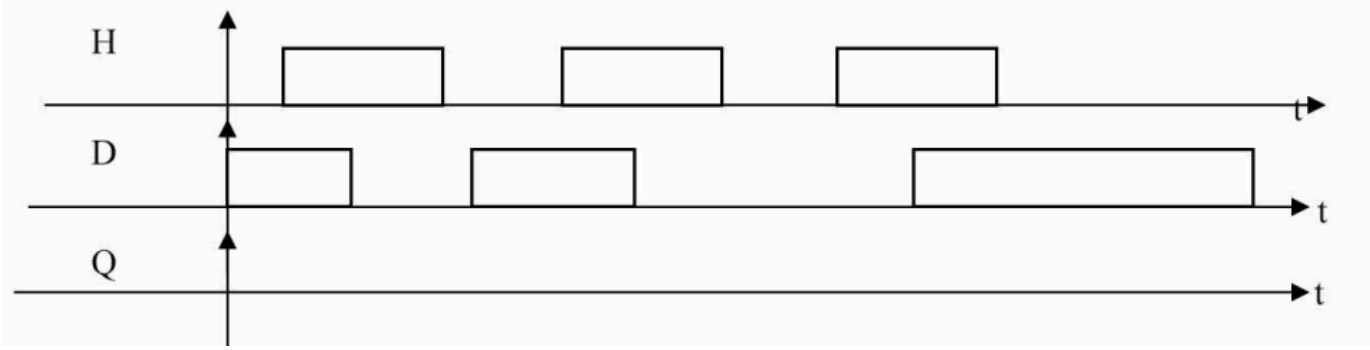
2- Complete the chronogram of the SRT latch synchronized on the high level of T.



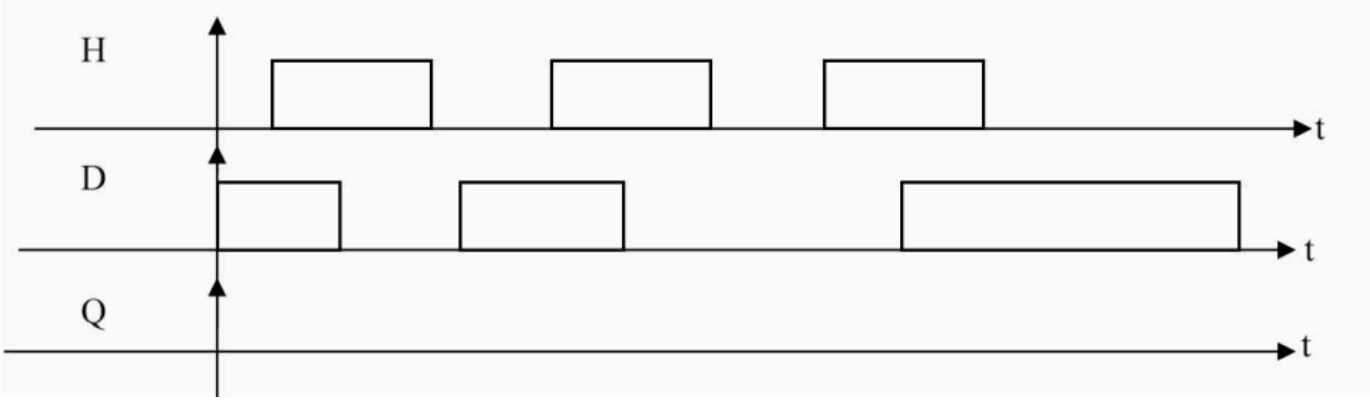
Exercise 2:

1- Complete the chronogram determining the operation of the D latch for each case where the latch responds to the synchronizations of the designated clock signal.

Latch D/ Low level of H



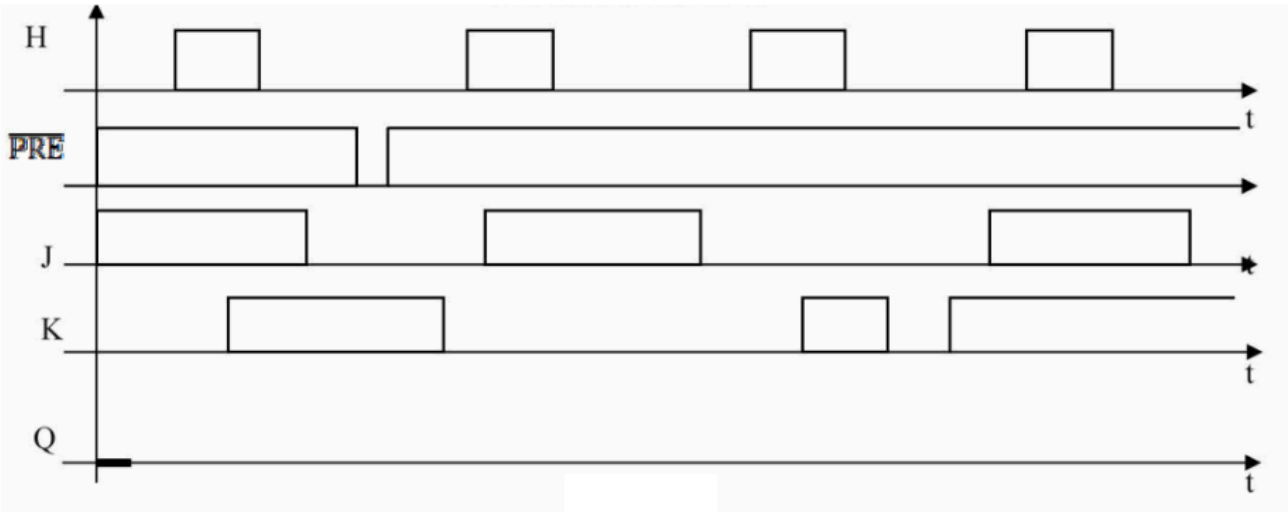
Latch JK / Rising edge of H



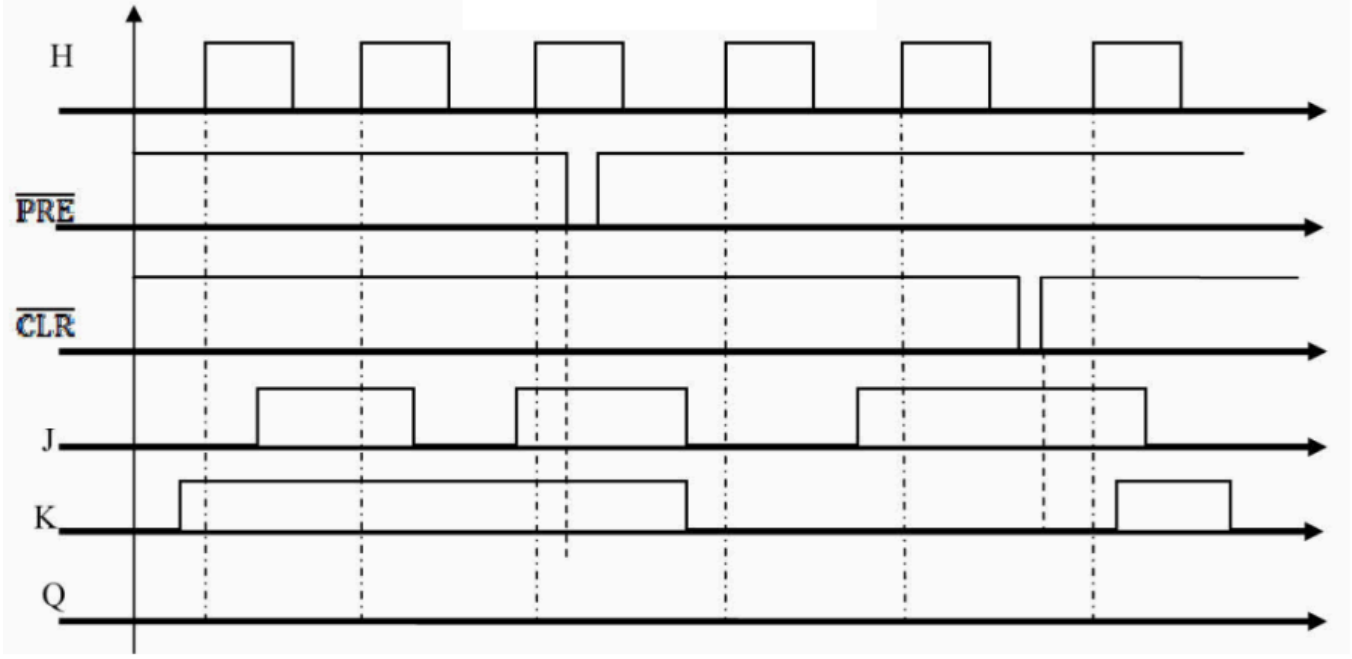
Exercise 3:

Complete the chronogram associated with the synchronized JK latch as follows:

Latch JK / Low level of H

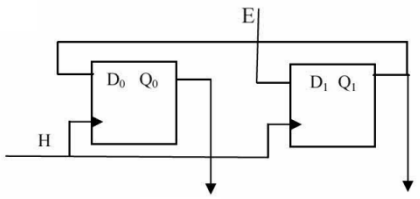


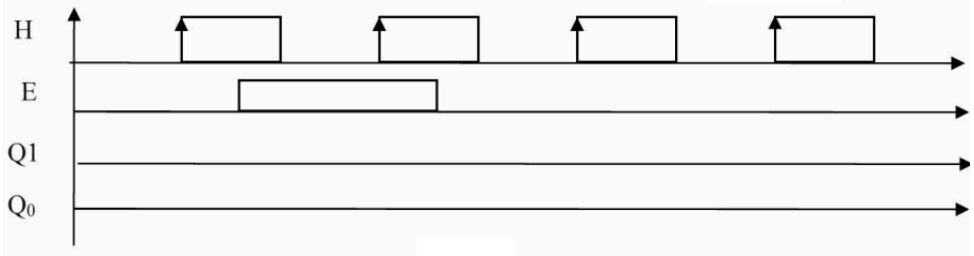
Latch D/ Descending edge of H



Exercise 4: Consider the circuit shown in the following figure:

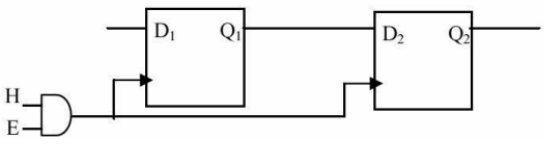
1- Complete the chronogram associated with this circuit.
2- Deduce the role of this circuit.

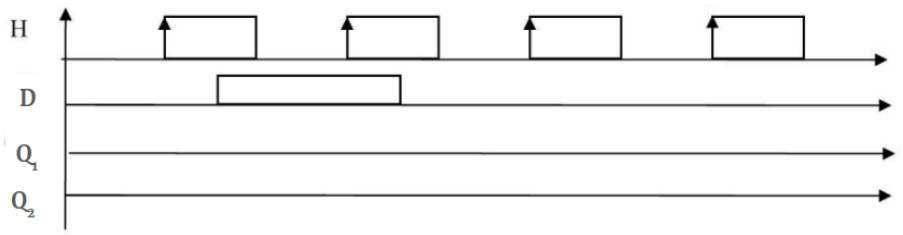




Exercise 5: Consider the circuit shown in the following figure:

1- Complete the chronogram associated with this circuit (for each case of E).
2- Deduce the role of this circuit (for each case of E).





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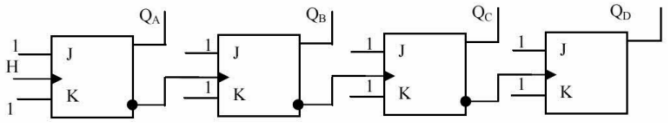
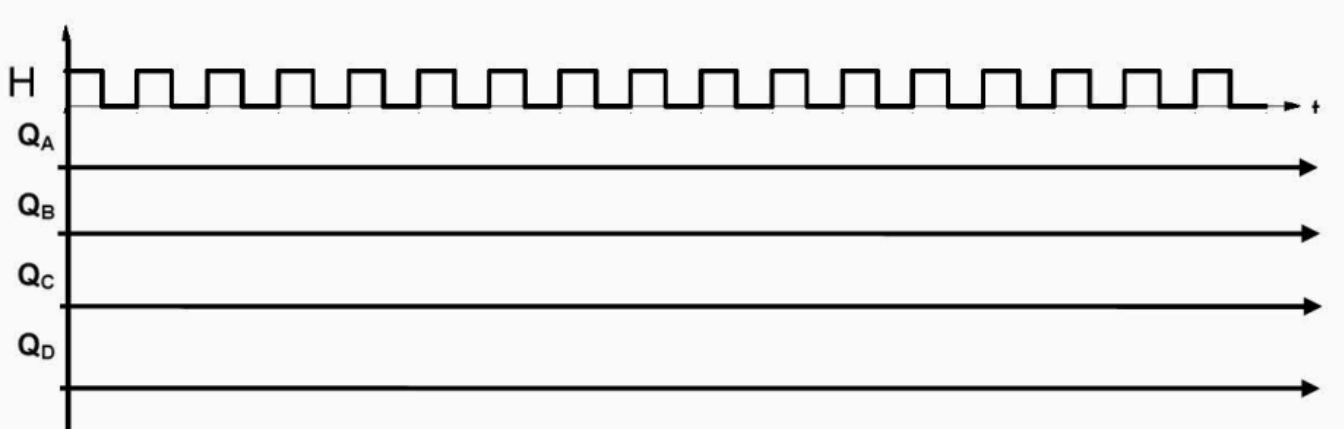
Exercise 6:

Considering the following implementation:

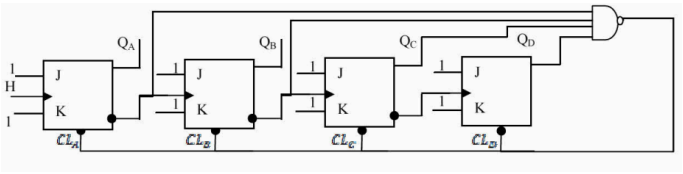
1- Complete the chronogram associated with this circuit and deduce the role of this circuit.





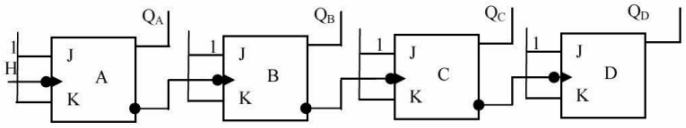
2- By slightly modifying the implementation of the previous figure, we obtain the implementation illustrated in the following figure:

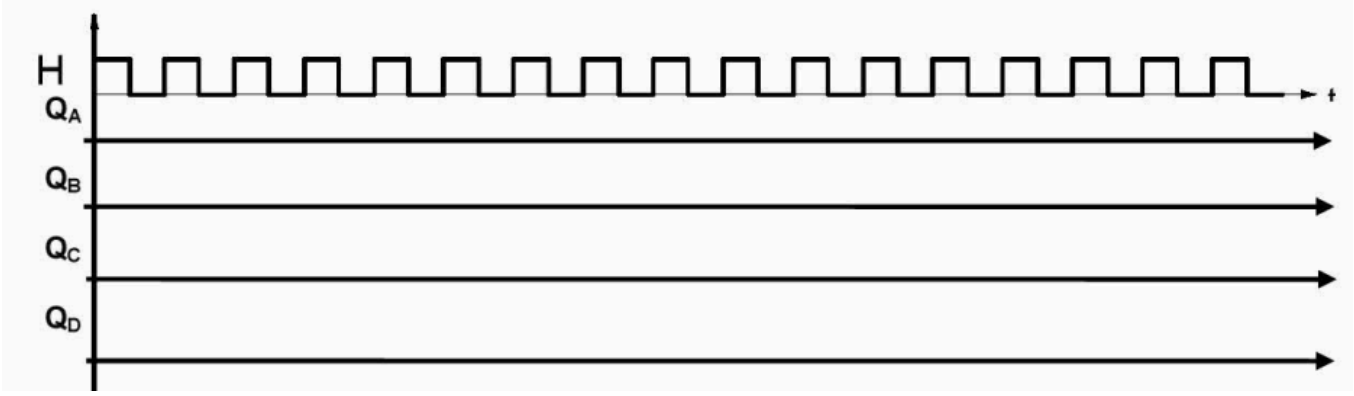
- what does this circuit achieve (justify your answer)



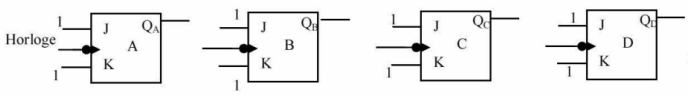
3- Considering the following implementation:

- Complete the chronogram associated with this circuit and deduce the role of this circuit.





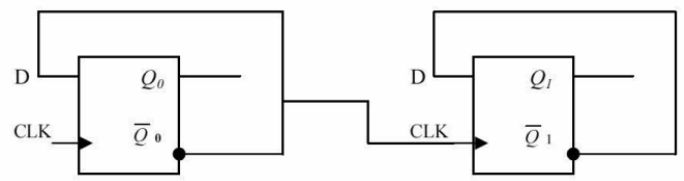
4- Wire the implementation from the previous figure to achieve an asynchronous modulo-14 counter

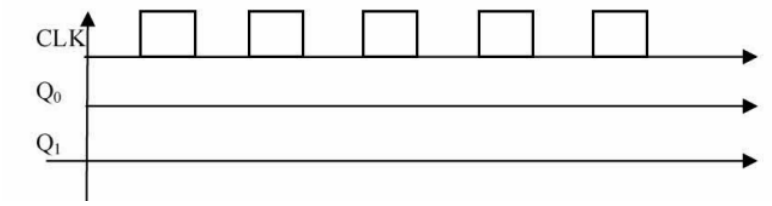


Exercise 7:

Considering the following circuit:

1- Complete the chronogram associated with this circuit



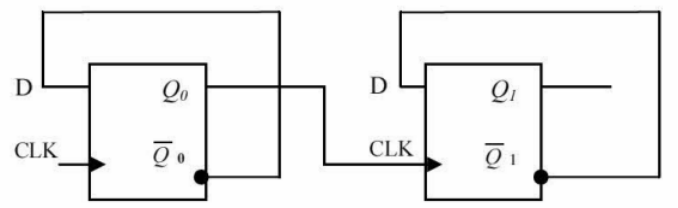


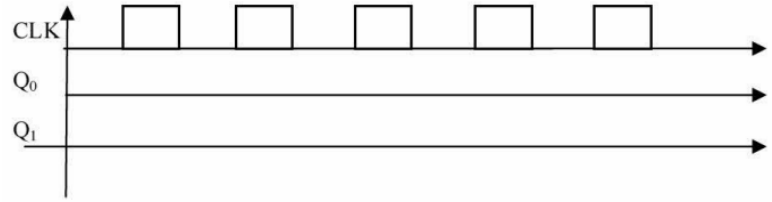
2- What is the sequence of output signals obtained? and what is the function performed?

3- Study and give the diagram of a modulo 8 asynchronous counter with D latch?

4- Considering the new circuit:

- Complete the chronogram associated with this circuit





5- What is the sequence of output signals obtained? and what is the function performed?

6- Study and give the diagram of a modulo 8 asynchronous decrement counter with D latch?